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reset input clk reset output rand wire
rand reg 3 0 temp always posedge reset
begin temp

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implementation is relatively simple a
shift register with a number of terms
xord together to create the feedback
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prbs pseudorandom binary code or
pseudorandom bitstream is a binary
sequence that while generated with a
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that i have tried different combinations
as shown in the code and
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occurring with the same

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here are the key lines of code for a 19
bit lfsr which generates a prbs the
output is simply lfsr bit 0 code reg 18 0
lfsr 0 always

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